A V-Band Quasi-Optical GaAs HEMT Monolithic Integrated Antenna and Receiver Front End

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***Abstract*—A single-chip monolithic integrated V-band folded-slot antenna with two Schottky-barrier diodes and a local oscillator source is developed as a quasi-optical receiver for the first time. The monolithic microwave integrated circuit consists of a voltage-controlled oscillator (VCO), a coplanar waveguide (CPW)-to-slotline transition, a low-pass filter, a folded-slot antenna, and a 180° single balanced mixer. The chip is fabricated based on the 0.15-μm GaAs high electron-mobility transistor technology and the overall chip size is 3×1.5 mm^2. A finite-difference time-domain method solver is also developed for analyzing the embedded impedance characteristics of the folded-slot antenna to design the mixer. The chip is placed on an extended hemispherical silicon substrate lens to be a quasi-optical receiver. The performance of the receiver is verified by experimental measurements. The VCO has achieved a tuning range from 61.9 to 62.5 GHz and approximately 9.3-dBm output power. The CPW-to-slotline transition has bandwidth from 50 to 70 GHz. The mixer results in 15-dB single-sideband conversion loss and the receiving patterns of the IF power are also measured.**

***Index Terms*—Coplanar waveguides (CPWs), monolithic-microwave integrated-circuit (MMIC) mixers, MMIC oscillators, slot antennas, slotline.**

I. Introduction

THE quasi-optical mixer is a useful device, which combines the functions of a receiving antenna and a mixer together, for efficiently transforming the high-frequency space wave to the low-frequency guided wave very near the antenna. In millimeter-wave applications, the mixer or detector can be attached directly to the antenna to avoid the mechanical complexity and the feed losses of the conventional RF feed distribution network. Furthermore, the distribution network can be incorporated at a much lower frequency where losses are lower and circuit dimensions are not critical. Recently, several quasi-optical mixers designed at various frequencies have been introduced [1]–[8]. Self-contained receivers at X-band were formed in [1] by integrating a coupled slot antenna, Schottky diode balanced mixer, and Gunn diode or a MESFET local oscillator (LO) source. X-band quasi-optical receivers that employed a coupled slot antenna and a balanced high electron-mobility transistor (HEMT) or MESFET self-oscillating mixer were presented in [2]. The design and modeling of a quasi-optical monolithic mixer made up by a slot-ring antenna with two Schottky diodes at X-band was described in [3]. The effect of orthogonal modes in a folded-slot antenna fed by slotline and coplanar waveguide (CPW) on opposite sides was investigated in [4] and the quasi-optical mixer realized by two diodes mounted in the slots of the antenna to provide mixing between the received RF and injected LO signals was shown in [5] at X-band. A quasi-optical mixer realized as a resistive heterostructure field-effect transistor (HFET) mixer with an integrated slot antenna at 40 GHz was presented in [6]. A 90-GHz Schottky diode receiver based on a double-slot antenna fed by a CPW was presented in [7]. A modified rectangular loop slot antenna was introduced as an alternative to the twin-slot antenna at 65 GHz in [8]. In [3], [5]–[8], external LO circuits were required for the mixers. In [3] and [6]–[8], a waveguide horn was used to irradiate LO power to the mixers. This technique involves substantial loss of LO power [1]. In [5], the LO signal was fed by a waveguide from external LO circuits. Limited by the small dimensions, this LO feeding network is difficult to realize at millimeter wavelength.

In this paper, a V-band self-contained quasi-optical integrated receiver is proposed as an improved design. A folded-slot antenna and a balanced Schottky diode mixer with an HEMT voltage-controlled oscillator (VCO) built on the same monolithic GaAs chip is realized. For the mixer design, a general full-wave analysis technique based on the finite-difference time-domain (FDTD) method is developed. The technique utilizes perfectly matched layer absorbing boundary condition [9], which allows more accurate modeling of the radiation boundary condition. The embedding impedances at different positions of the folded-slot antenna are calculated by the unit cell excitation model. The results are compared with the simulated impedance results of the diode to design the mixer. A VCO is designed based on a 0.15-μm HEMT technology to provide the source of LO signal using a similar circuit architecture reported in [10]. A reduced-size CPW-to-slotline transition is designed based on the concept proposed in [11] for the LO pumping network. The resulting receiver is placed on an extended hemispherical silicon lens to eliminate the power loss of the substrate mode and increase the gain of the RF signal [12]. The silicon lens is chosen due to its high dielectric constant close to the GaAs substrate. From the measurement results, approximately 9-dBm LO power output from the VCO is injected to the integrated antenna mixer through the CPW-to-slotline transition, which has bandwidth from 50 to 70 GHz. Approximately 15-dB single-sideband isotropic conversion loss is achieved excluding the gain of the dielectric lens. This monolithically integrated self-contained receiver chip could be suitable for detector or

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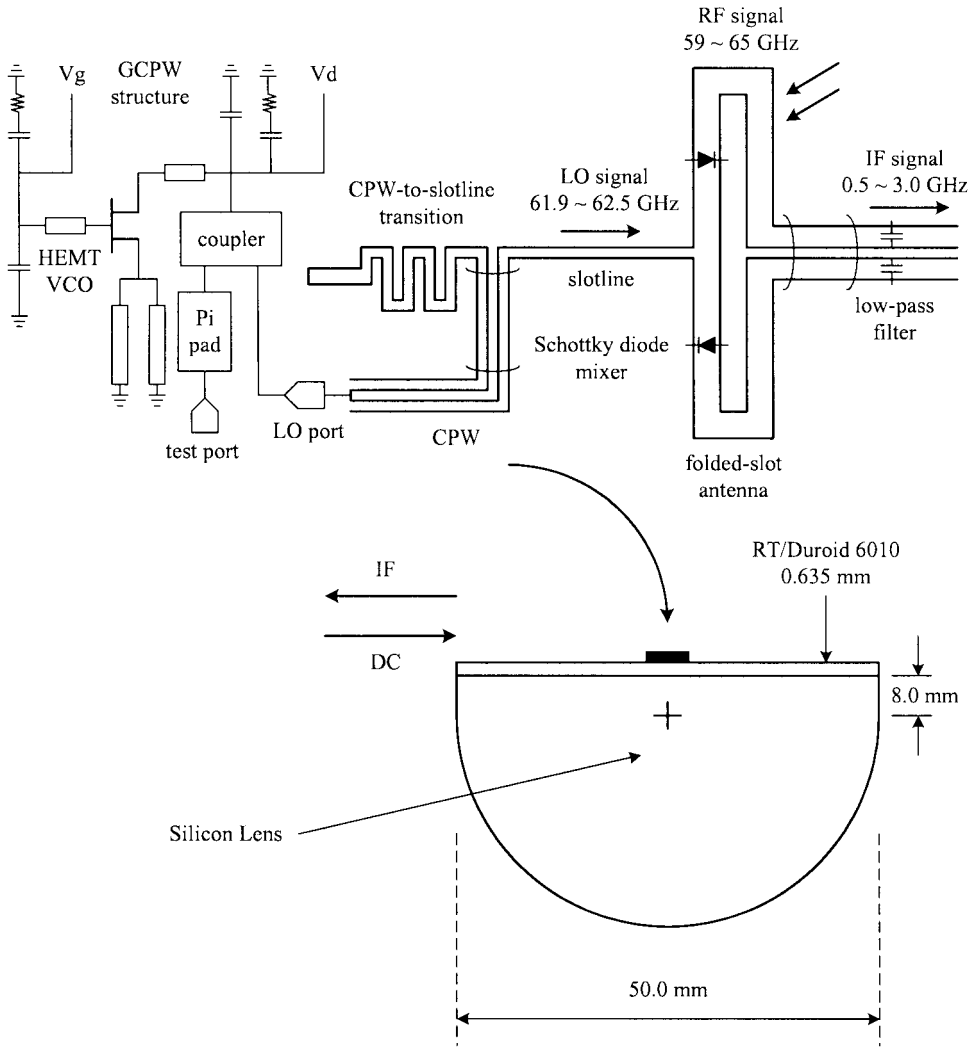

Fig. 1. Schematic diagram of the quasi-optical integrated antenna and receiver front end.

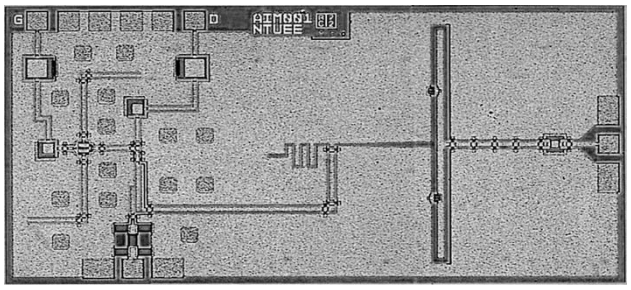

Fig. 2. Chip photograph of the integrated antenna and receiver front end.

sensor applications where compact size and light weight are required.

II. Integrated Antenna Mixer Design

The architecture and photograph of the folded-slot balanced mixer are shown in the right-hand sides of Figs. 1 and 2, respectively. Two diodes are mounted in the slot of the antenna to mix the LO signal injected from the slotline and RF signal received by the antenna. It is worth mentioning that, although the coupled slot antenna used in [1] and [2] has the particular even-/odd-mode characteristic for receiving space wave and propagating guided wave at the same time, which makes it possible to be the receiving antenna and 180° balun at the same time for designing the integrated antenna mixer, the folded-slot antenna [4] preserves this property and only planar structures are used [5]. Another planar slot-ring antenna can also be used to achieve the 180° single balanced integrate antenna mixer with an LO signal injected from the space wave in polarization orthogonal to the RF signal [3]. The double-slot antenna used in [7] and the modified rectangular loop slot antenna used in [8] could be designed to have symmetrical E- and H-plane patterns. However, when dielectric lens is applied to suppress the substrate mode and to enhance the gain, the pattern of folded-slot antenna is also nearly symmetrical in the E- and H-plane. For these reasons, we choose the folded-slot antenna to monolithically integrate the antenna, mixer, and LO source in a single chip.

The RF signal received by the antenna and the LO signal generated by the VCO are mixed by two diodes mounted in the slot of the folded-slot antenna. The parameters that could be adjusted for matching the diode to the RF and LO signals are the size of the diodes, location of the diodes, and dimensions of the antenna. The scaled model of the two-finger 30-μm diode is

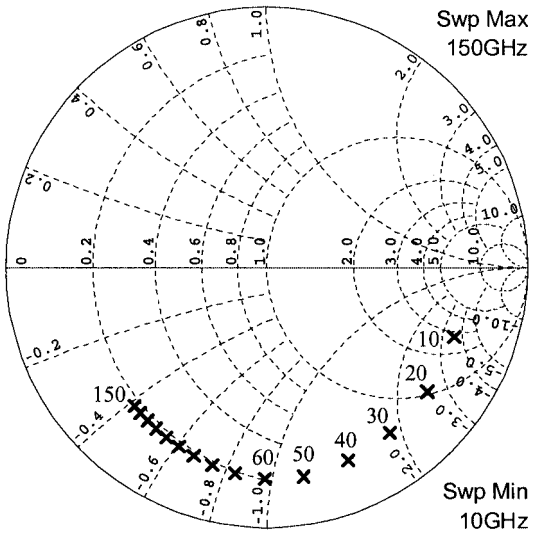

Fig. 3. Simulated impedance of Schottky-barrier diode.

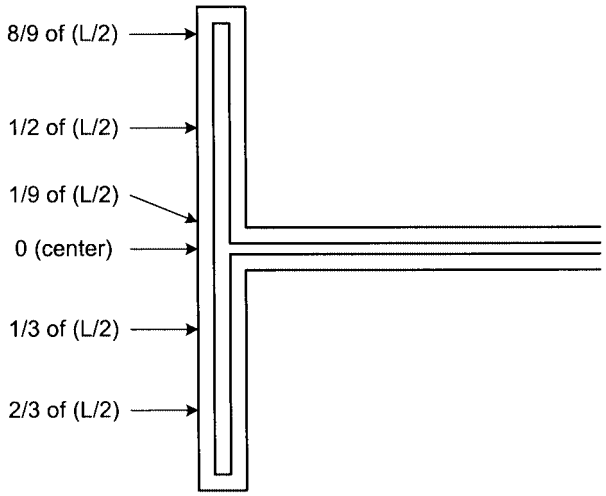

Fig. 4. Various positions of folded-slot antenna.

simulated by the circuit design software Libra HP EEsof. Fig. 3 plots the simulation results with an LO power set at 6 dBm and the frequencies swept from 10 to 150 GHz. At 60 GHz, the diode can be modeled as an RC series connection equivalent circuit, where $R = 10\ \Omega$ and $C = 0.05$ pF. To optimize the design of the mixer, the location of the diodes and the dimensions of the antenna are varied and simulated by a FDTD full-wave solver. Although the CPW-fed folded-slot antenna has previously been investigated by the FDTD method in [13], no embedding impedance data is available at the various positions shown in Fig. 4. The embedding impedance of the folded-slot antenna at the location where diodes are mounted is a major concern of our integrated antenna mixer design. In our analysis, the perfectly matched layer absorbing boundary condition proposed in [9] is applied to accurately model the radiation boundary condition. The unit cell excitation model [14], which is capable of calculating the impedance seen by a point source, is also adapted in the analysis. Both the voltage and current information are recorded in the time domain and transformed into the frequency domain to obtain the impedance results. Since the quasi-optical receiver will be mounted on the planar surface of a dielectric lens, which is electrically large, the antenna element will act as if it is at the interface of an air–dielectric half-space. Thus, the simulation environment is a half-space GaAs substrate in which the antenna is printed at the interface. It is worth mentioning that a symmetrical excitation of the folded-slot antenna is needed to avoid the convergence problem caused by the nonradiation mode. Fig. 5 plots the simulated embedding impedances of the folded-slot antenna at various positions measured from the center of the slot. Besides matching the impedance between the diodes and folded-slot antenna, the return loss of the injected LO signal is another major concern. In general, the RF signal is much smaller than the LO signal such that it is important to design the circuit for diodes matched to the LO signal. The lumped-element modeling technique in [14] is employed here to calculate the return losses at the LO port by changing the location of the diodes. The results are shown in Fig. 6. In obtaining Fig. 6, the diodes are placed symmetrically about the LO feeding slotline. From the simulation data, the best result is at the middle from the center to the edge of the slot. The length of the folded-slot antenna is chosen to be 1250 μm, which is a quarter of free-space wavelength at 60 GHz. It should be noted that there are some factors, such as the effect due to the IF line and the existence of the real diodes, that may cause error between actual and simulated results.

The IF frequency is from 0.5 to 3.0 GHz, which is much lower than the RF and LO frequency, so it is impractical to make a low-pass filter (LPF) by waveguide sections on the chip as that described in [5]. Instead, an on-chip LPF is implemented by a 0.5-pF shunt capacitor.

III. V-Band VCO and CPW-to-Slotline Transition Design

The schematic diagram and photograph of the V-band VCO are shown in the left-hand side of Figs. 1 and 2, respectively. Since the LO power affects the mixer conversion loss before the saturation phenomenon occurs, the VCO is designed for output power consideration. A four-finger 200-μm HEMT device is used. The summation of reactances looking in and out from the drain terminal calculated by the device linear model was set to zero at the oscillation frequency, while the negative resistance looking into the drain terminal was chosen to obtain high output power. The oscillation frequency is adjusted by changing the gate voltage, and the output power is coupled out of the drain terminal via a coupler. Metal–insulator–metal (MIM) capacitors are employed for oscillation signal bypass. Resistors and capacitors are used in the bias networks. All the passive structures are characterized by the full-wave electromagnetic (EM) analysis. The VCO is designed on a grounded coplanar waveguide (GCPW) structure to make the circuit accommodate to the integrated antenna mixer structure. Since the VCO is built on the same chip and very close to the antenna, the GCPW is used instead of a CPW to prevent the VCO from being injection locked to the RF signal. The coupler is formed by edge-coupled GCPW lines to have a dc blocking property and designed to transform the load impedance at the LO port to the designed impedance at the drain terminal. The coupler

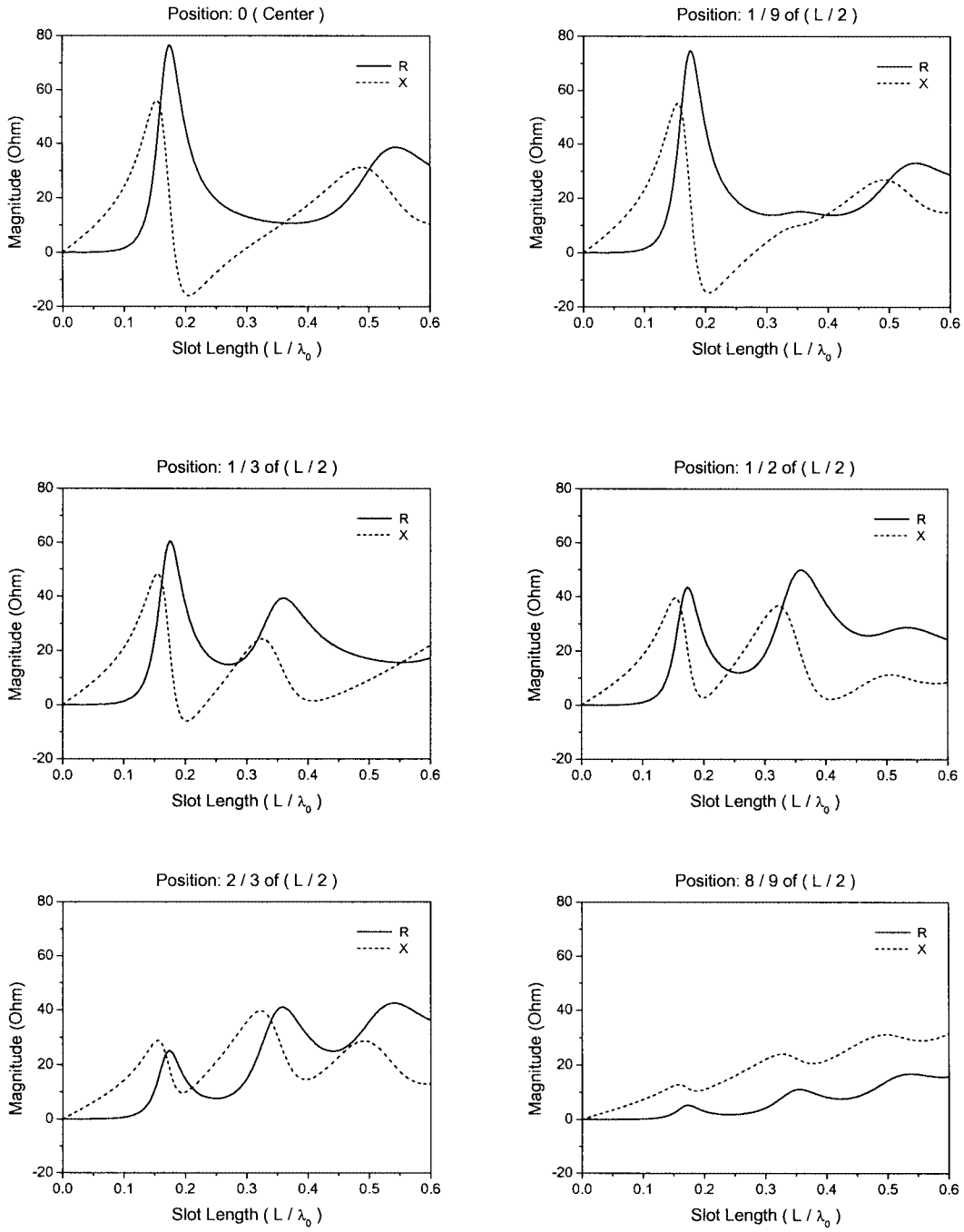

Fig. 5. Simulated embedding impedances of folded-slot antenna at various positions.

has 6-dB insertion loss at the LO port and 10-dB insertion loss at the test port. The Pi pad, which has 14-dB attenuation, is implemented before the test port as an isolator. A test port is used here to test the VCO operating frequency and the output power. The test port will be left open when measuring the integrated antenna mixer so an isolator is needed to suppress the influence. Besides the antenna integrated receiver chip, an additional VCO test circuit is also fabricated for characterizing the performances of the VCO alone.

The structure of the CPW-to-slotline transition is shown in the middle area of Fig. 1. The transition is needed for the connection between the LO output port of the VCO and the slotline that feeds the LO power into the integrated antenna mixer. Since the tuning range of the VCO is limited to 1 GHz, the transition is designed for size consideration. To reduce the size, a planar LC circuit composed of an interdigitated capacitor and a shorted slotline stub is utilized to replace the conventional $\lambda/4$ transformer structure in [11]. Based on the same design principle, the lumped-element CPW-to-slotline transition is implemented in V-band. The dimension parameters are tuned for designing the center frequency at 60 GHz. In order to characterize the performance of such a transition, another test circuit consisting of the back-to-back connection of two such transitions is also fabricated.

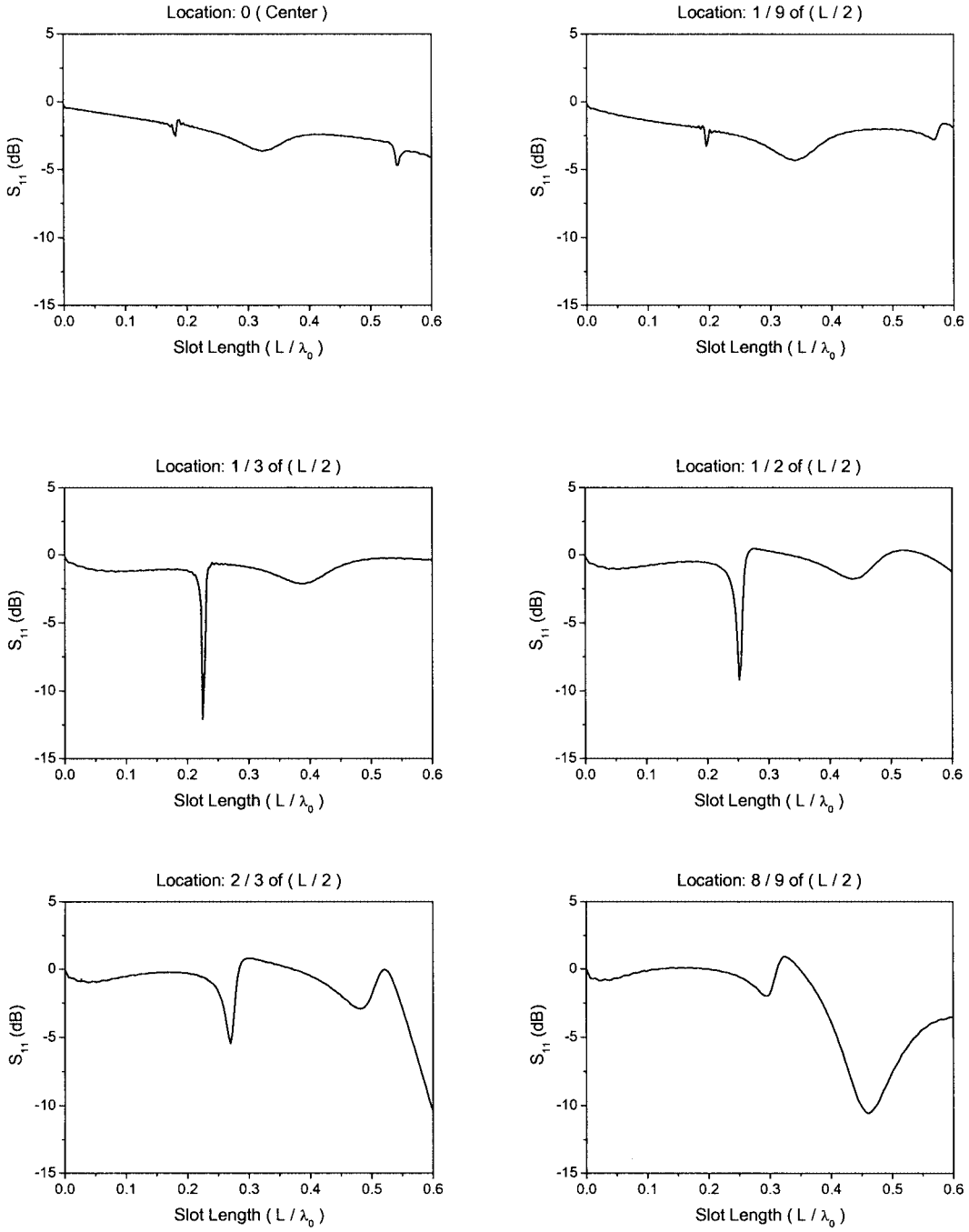

Fig. 6. Simulated return losses of LO input port for diodes placed at various locations.

IV. Simulation and Measurement Results

Two VCO test circuits were measured from the LO port by the probe station with Cascade Microtech wafer probes and the spectrum analyzer Agilent 8565EC. Fig. 7 plots the oscillation frequency and output power as functions of the bias current for both test circuits. The bias voltage V_d is fixed at 4 V and voltage V_g varies for tuning the bias current. The gate control tuning range of the oscillation frequency is from 63.5 to 62.5 GHz. The maximum output power is over 11 dBm. Four CPW-to-slotline transition test circuits were also measured via on-wafer probing and via the network analyzer HP 8510C with very similar results. Fig. 8 plots the measured S-parameters of one test circuit. The return losses S_{11} and S_{22} are over 10 dB from 50 to 70 GHz. The insertion losses S_{21} and S_{12} are less than 0.7 dB in the same frequency band. The measured center frequency agrees well with the simulation.

The performance of the VCO included in the integrated receiver chip is measured from the test port in the same way as the VCO test circuits. Since the coupler has 6-dB insertion loss at the LO port and 10-dB insertion loss at the test port, the Pi pad, which has 14-dB attenuation, is implemented before the test port as an isolator, the output power level at the LO port is estimated as 18 dB higher than the measured power level at the test port. Fig. 9 plots the oscillation frequency and LO port output power level as functions of the bias tuning voltage V_g. The frequency

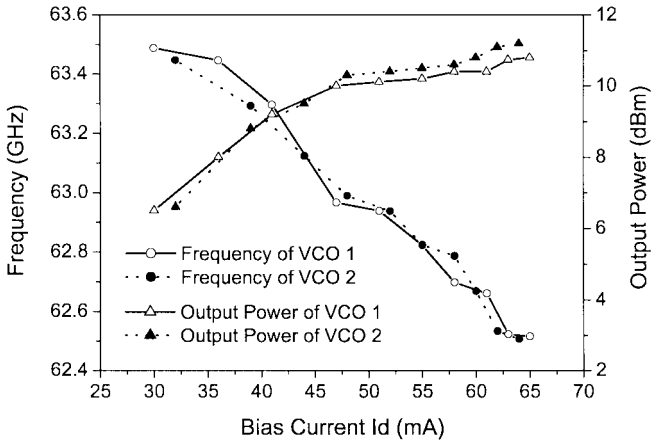

Fig. 7. Measured oscillation frequency and output power of the VCO test circuits.

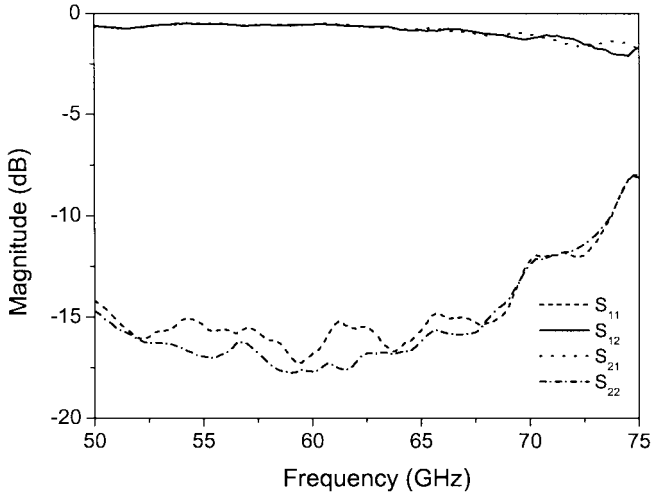

Fig. 8. Measured S-parameters of the CPW-to-slotline transition test circuit.

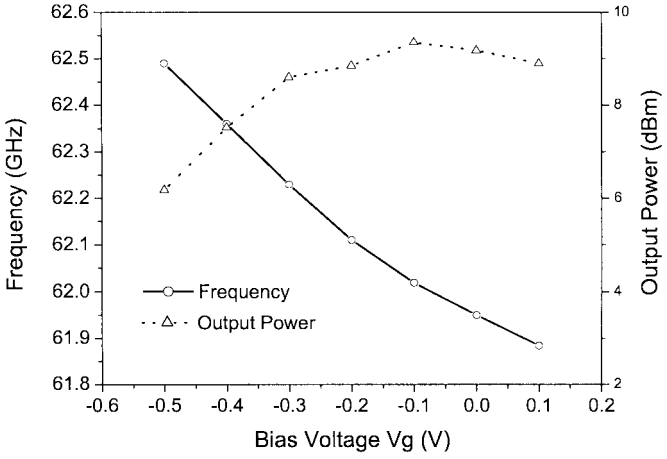

Fig. 9. Measured oscillation frequency and output power at the LO port as functions of gate voltage.

tuning range is from 62.5 to 61.9 GHz and the output power is from 6.2 to 9.3 dBm. The results are different from those obtained in a single VCO test circuit. The load impedance at the LO port in the integrated receiver chip could be different from the probe termination impedance (50 Ω) and the difference

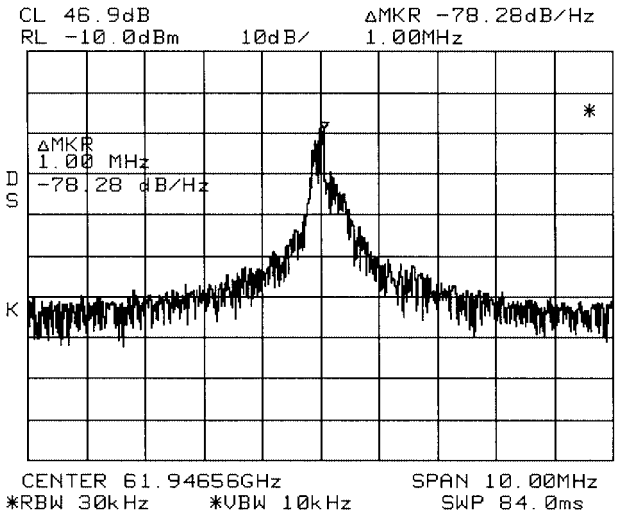

Fig. 10. Spectrum analyzer plot of the VCO measured at the test port.

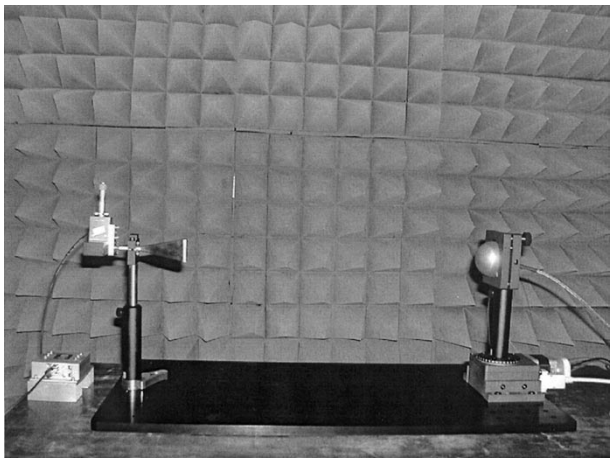

Fig. 11. Setup for measuring the quasi-optical receiver.

causes the deviations of oscillation frequency and output power level. A phase noise of approximately -78.28 dBc/Hz for an offset frequency of 1 MHz is read from the spectrum analyzer plot, as shown in Fig. 10.

The GaAs chip with dielectric constant $\varepsilon_r = 12.9$ is mounted onto an RT/Duroid 6010 substrate of dielectric constant $\varepsilon_r = 10.2$, as shown in Fig. 1. The silicon lens diameter is 50.0 mm, which is approximately ten times of the free-space wavelength at 60 GHz. The extension length is chosen to be 8.0 mm for providing 23-dB gain with 90% Gaussicity (pattern coupling efficiency) from the dielectric lens [12]. The photograph of the measurement setup is shown in Fig. 11. A V-band standard gain horn antenna is used to irradiate the RF signal to the quasi-optical receiver. The VCO is operating at 62.0 GHz. The IF signal is picked out from the chip through the bond wires connecting the pads on the chip and the CPW line on the printed circuit board. A subminiature A (SMA) connector and a coaxial cable are used to guide the IF signal from the printed circuit board to the spectrum analyzer. The isotropic conversion loss [1] is used to characterize the receiver chip. The reference RF power is the power that would be received by a fictitious isotropic antenna at the same measurement condition as the

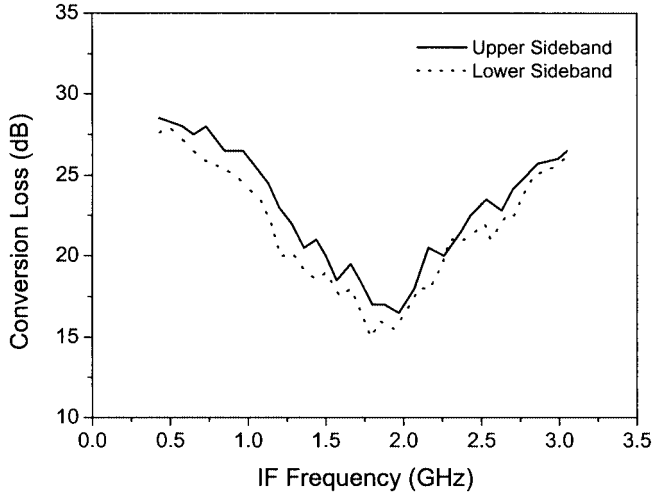

Fig. 12. Receiver chip isotropic conversion losses of upper and lower sideband signals versus IF frequency.

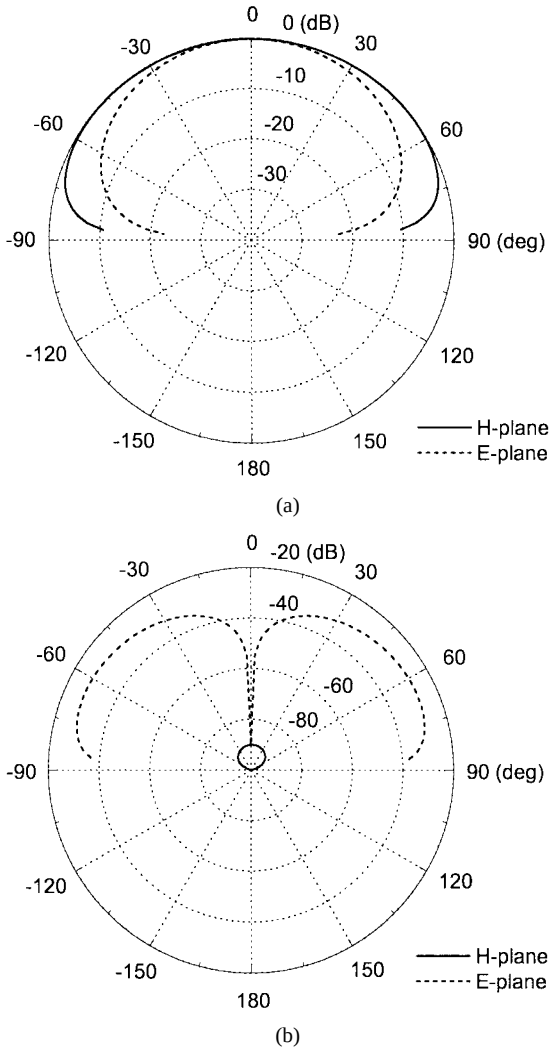

Fig. 13. Computed radiation patterns inside the lens. (a) Co-polar H- and E-plane patterns. (b) Cross-polar H- and E-plane patterns.

receiver chip. Fig. 12 plots both the upper and lower sideband isotropic conversion losses. The conversion losses of both sidebands decrease first to a minimum level as the IF frequency

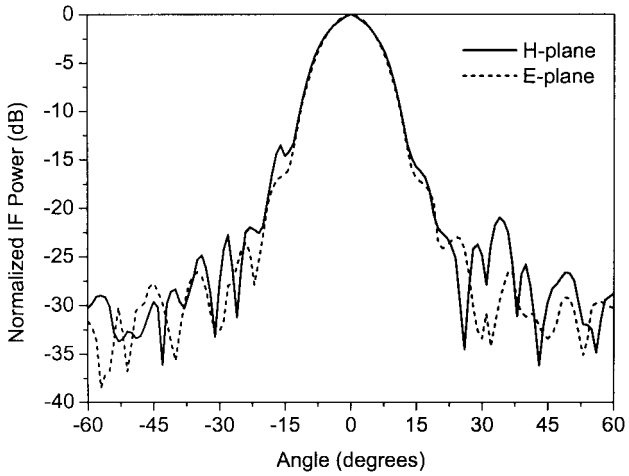

Fig. 14. Measured normalized IF power patterns of the quasi-optical receiver under co-polar receiving condition.

increases and then increase as the IF frequency increases. The receiving patterns of the quasi-optical receiver are then measured at 1.7 GHz where maximum IF power is obtained. The simulated co-polar and cross-polar radiation patterns inside the lens are shown in Fig. 13. The cross-polarization level is small compared to the co-polarization level. The normalized IF power receiving patterns are shown in Fig. 14. The H- and E-plane patterns are symmetrical with high-directivity and low-sidelobe levels.

V. Conclusions

A V-band monolithic integrated quasi-optical receiver has been designed and demonstrated for the first time. The LO source provided by the on-chip VCO has been included in the design for a self-contained integrated antenna mixer. Over 9-dBm VCO output power around 60 GHz has been obtained by 0.15-μm GaAs HEMT technology. The embedding impedance of the folded-slot antenna has been investigated by the FDTD method with a unit cell excitation model and compared with the simulated diode impedance to optimize the mixer design. Approximately 15-dB single-sideband isotropic conversion loss has been achieved, excluding the gain of the silicon lens. These results show the potential of the chip to be operated as a detector, sensor, or digital modulated signal receiver.

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